IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An electronic assembly comprising:

a substrate;

a die; and

a plurality of interconnections between the substrate and die;

wherein respective ones of the interconnections include

a relatively low melting temperature and yield strength reflowed solder bump on the die, a relatively higher melting temperature and electrically conductive material standoff on the substrate in the form of a stiff bump extending above a [[the]] substrate surface and having a yield strength in the 350-450 MPa range, and

a soldered joint connection between ~~connecting~~ the reflowed solder bump and [[to]] the electrically conductive material standoff.

2. (Canceled)

3. (Currently Amended) The electronic assembly according to claim 1, wherein a [[the]] top surface of the standoff is wetted by the reflowed solder bump to form the soldered joint connection.

4. (Currently Amended) The electronic assembly according to claim 1, wherein the standoff is a bump in [[the]] a form of a column or stud.

5. (Currently Amended) The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material standoff [[is]] includes copper.

6. (Canceled)

7. (Currently Amended) The electronic assembly according to claim 1, wherein the die has an inter layer dielectric material under the plurality of interconnections.

8. (Canceled)

9. (Currently Amended) The electronic assembly according to claim 1, wherein [[the]] a coefficient of thermal expansion of the substrate is at least 15 ppm/°C and [[the]] a coefficient of thermal expansion of the die is at least 2.7 ppm/°C less than that of the substrate.

10. (Currently Amended) The electronic assembly according to claim 1, wherein [[the]] a coefficient of thermal expansion of the substrate is more than two times greater than [[the]] a coefficient of thermal expansion of the die.

11. (Currently Amended) A semiconductor package comprising:

a package substrate having a coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of relatively high melting temperature and electrically conductive standoff contact members on the substrate; and

a die having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than that of the substrate, a front side of the die having a plurality of relatively lower yield strength reflowed solder bumps thereon, wherein the solder bumps are plastically deformed, the die being electrically coupled to ~~located on~~ the substrate with a soldered joint connection between each of the solder bumps and a ~~connected to the~~ respective one [[ones]] of the standoff contact members ~~by soldered joints electrically coupling the die to the substrate~~.

12. (Original) The semiconductor package according to claim 11, wherein the coefficient of thermal expansion of the substrate is more than twice that of the die.

13. (Currently Amended) The semiconductor package according to claim 12, wherein the standoff contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein each of the soldered joint connections ~~joints~~ connect the die to [[the]] tops of respective ones of the standoff elements.

14. (Currently Amended) The semiconductor package according to claim 13, wherein the standoff elements are non-melting at a [[the]] solder liquidous temperature.

15. (Original) The semiconductor package according to claim 13, wherein the standoff elements are copper bumps.

16. (Currently Amended) The semiconductor package according to claim 13, wherein each solder bump ~~the soldered joints each comprise solder on the die which~~ is wetted onto a surface of the respective [[a]] contact member of the substrate to form the soldered joint connection.

17. (Currently Amended) The semiconductor package according to claim 11, wherein the die has an inter layer dielectric material under the solder joint connections ~~thereon~~.

18-26. (Canceled)

27. (Currently Amended) A semiconductor package comprising:

a package substrate having a plurality of relatively high melting temperature and electrically conductive standoff contact members on the substrate each in the form of a stiff bump extending above a substrate surface and having a yield strength in the 350-450 MPa range; [[and]]

a die having a front side with a plurality of relatively low melting temperature and yield strength reflowed solder bumps thereon[[,]]; and

a soldered joint connection between each of the plurality of reflowed solder bumps of the die and respective ones of the plurality of standoff contact members of the substrate. ~~the die capable of being coupled to the substrate with the solder bumps connected to the respective ones of the standoff contact members by soldered joints electrically coupling the die to the substrate~~.

28. (New) The electronic assembly of claim 1 wherein the solder bump includes a stress-relieving element to absorb stress in the plurality of interconnections.

29. (New) The electronic assembly of claim 1 wherein the reflowed solder bump has a solder reflow finish.

30. (New) The electronic assembly of claim 1 wherein the solder bump is plastically deformed.

31. (New) The electronic assembly of claim 1 wherein the solder bump comprises at least one of lead, silver and tin.

32. (New) The semiconductor package of claim 11 wherein each of the plurality of solder bumps includes a stress-relieving element to absorb stress.

33. (New) The semiconductor package of claim 11 wherein each of the plurality of solder bumps has a solder reflow finish.

34. (New) The semiconductor package of claim 11 wherein each of the plurality of solder bumps comprises at least one of lead, silver and tin.

35. (New) The semiconductor package of claim 27 wherein each of the plurality of solder bumps includes a stress-relieving element to absorb stress.

36. (New) The semiconductor package of claim 27 wherein each of the plurality of solder bumps has a solder reflow finish.

37. (New) The semiconductor package of claim 27 wherein each of the plurality of solder bumps comprises at least one of lead, silver, and tin.

38. (New) The semiconductor package of claim 27 wherein each of the plurality of solder bumps are inelastically deformed.

39. (New) A package comprising:

a die with multiple reflowed solder die bumps; and

a substrate with multiple contact members having a melting temperature higher than a melting temperature of the solder die bumps and having a yield strength in a range of about 350 MPa to about 450 MPa, wherein the multiple contact members are coupled to respective solder die bumps, and wherein the solder die bumps have a relatively lower yield strength than the multiple contact members.

40. (New) The package of claim 39 wherein the solder die bumps are inelastically deformed.

41. (New) The package of claim 39 wherein each of the solder die bumps includes a stress-relieving element to absorb stress.

42. (New) The package of claim 39 wherein each of the solder die bumps has a solder reflow finish.

43. (New) The package of claim 39 wherein the solder die bumps comprise at least one of lead, silver, and tin.